The Maharaja Sayajirao University of Baroda
Polytechnic
Diploma in Electronics & Communication Engg. (HPP)

ACADEMIC YEAR
2023-24

Year	III	**VLSI TECHNOLOGY(ELE3631)**	Lecture /Lab Hrs per week	4/2
Semester	II		Max marks	100

Pre-Requisite: Basic Electronics, Digital electronics

CO1	Explain VLSI design methodologies, design flow, hierarchy, regularity, modularity, locality, and CMOS fabrication.
CO2	Describe MOS structure, MOSFET operation, IV characteristics, scaling, and capacitances.
CO3	Analyze MOS inverters (resistive-load, NMOS-load, depletion/enhancement NMOS, CMOS) including delay and power.
CO4	Develop MOS logic circuits—CMOS logic gates, complex logic, sequential circuits, latches, flip-flops.
CO5	Implement FPGA/VHDL designs using behavioral and data-flow modeling.
BT	**1. Remember 2. Understand 3. Application 4. Analysis 5. Evaluation 6. Creation**

COURSE CONTENT/SYLLABUS

Unit	Unit Name	Hrs	Weightage	CO
1	INTRODUCTION TO VLSI DESIGN: Overview of VLSI design Methodologies, VLSI Design Flow, Design Hierarchy, Concepts of Regularity, Modularity, and locality, VLSI Design Styles, Design Quality, Fabrication Process Flow basic steps, CMOS n-well process	6	12	**CO1**
2	MOS TRANSISTOR : MOS structure, MOS system under external bias, Structure and operation of MOSFET transistor, MOSFET current-voltage Characteristics, MOSFET scaling and small geometry effects, MOSFET capacitances	6	12	**CO2**
3	MOS INVERTERS: Concept and working of MOS inverter, Resistive load Inverter, Inverter with n-type MOSFET Load, Enhancement load NMOS, Depletion Load, CMOS Inverter - circuit operation and description, Cascaded CMOS Inverter stages, Delay time, Switching power dissipation of CMOS Inverter.	10	18	**CO3**
4	MOS CIRCUITS: Combinational MOS Logic Circuits: MOS logic circuits with depletion NMOS load, CMOS logic circuits, Complex logic circuit, Sequential MOS Logic Circuit: Behaviour of bistable element, SR latch circuit, clocked latch and Flip-Flop circuit.	8	16	**CO4, CO3**
5	INTRODUCTION TO FPGA and VHDL FPGA structure, Types of FPGA, Signal delay in FPGA , Hardware Abstraction, Basic terminology, Entity declaration, Architecture body, Data objects, Data types, Operators	6	16	**CO5**
6	BEHAVIOURAL MODELING DATA FLOW MODELLING Entity declaration, Architecture body, Process statement, Variable and signal assignment statement, Wait, If, Case, Null, Loop, Exit, Next, Assertion, Report statement, Examples Concurrent signal assignment statement, conditional signal assignment statement, block statement, concurrent assertion statement, Examples	16	26	**CO5**
		52	**100**	

REFERENCE BOOKS:

1.	CMOS DIGITAL INTEGRATED CIRCUITS -Sung Mo Kang -TMH
2.	Circuit design with VHDL – Volnei A Pedroni - PHI
3.	VLSI Technology - Chang C.Y. and Sze S. M. - MGH
4.	VHDL design -J Bhaskar–Pearson